CLAIMS

What is claimed is:

1. A method of coupling a plurality of test access port (TAP) controllers to a single external interface, comprising: resetting a first bit in each of plurality of TAP controllers (102, 106) to a known state; producing a first signal based, at least in part, on the state of the first bit in each of the plurality of TAP controllers (102, 106); selecting one (108) of the plurality of TAP controllers based, at least in part, on the first signal; coupling an external input terminal to an input terminal of the selected one of the plurality of TAP controllers; and coupling an output terminal of the selected one of the plurality of TAP controllers to an external output terminal.

2. The method of Claim 1, wherein the TAP controller comprises a finite state machine and a plurality of registers.

3. The method of Claim 2, further comprising toggling the first bit in the selected one of the plurality of TAP controllers; and repeating steps (b) through (e).

4. The method of Claim 3, further comprising providing a clock signal, a test mode selection signal (104), and a test reset signal to each of the plurality of TAP controllers.

5. The method of Claim 3, wherein the plurality of TAP controllers are disposed on a single integrated circuit.

6. The method of Claim 5, wherein the first signal is produced within the single integrated circuit.

7. The method of Claim 6, further comprising receiving, from a source external to the single integrated circuit, a clock signal.

8. An integrated circuit, comprising: a plurality of functional blocks, each functional block having a test access port (TAP) controller coupled thereto; each TAP controller including a first register bit, each first register bit adapted to produce a known output state in response to a reset signal, each first register bit further adapted to toggle in response to a register write operation; and routing logic adapted to selectively provide, based at least in part on the state of the plurality of first register bits, a communication path between an external input signal source and an input terminal of a selected one of the TAP controllers.

9. The integrated circuit of Claim 8, wherein the routing logic is further adapted to selectively provide, based at least in part on the state of the plurality of first register bits,

a communication path between an external output terminal and an output terminal of the selected on the TAP controllers.

10. The integrated circuit of Claim 8, wherein at least one TAP controller further includes a second register bit; wherein the routing logic is further to provide the output of a first TAP controller as an input to a second TAP controller, based at least in part on the state of the first and second register bits.

11. The integrated circuit of Claim 9, wherein a transition between the selectively provided communication paths is transparent to an external observer.

12. An integrated circuit (IC), comprising: a plurality of TAP controllers disposed on the IC, each of the plurality of TAP controllers having a first input terminal adapted to receive a data input signal and an output terminal adapted to provide a data output signal, each of the plurality of TAP controllers further having at least one switch bit; a first interface to receive an externally supplied input signal; a second interface to transmit an internally generated output signal; routing logic adapted to selectively provide, based at least in part on the state of the switch bits of the plurality of TAP controllers, a first communication path between the input terminal of a predetermined one of the plurality of TAP controllers and the first interface, and a second communication path between the output terminal and the second interface.

13. The integrated circuit of Claim 12, further comprising a plurality of functional blocks coupled respectively to each of the plurality of TAP controllers.

14. The integrated circuit of Claim 13, wherein the each of the plurality of TAP controllers has a second input terminal adapted to receive a clock signal, a third input terminal adapted to receive mode select signal, and a fourth input terminal adapted to receive a reset signal; wherein the plurality of second input terminals are coupled in common, the plurality of third input terminals are coupled in common, and the plurality of fourth input terminals are coupled in common.

15. The integrated circuit of Claim 14, further comprising a chain bit disposed in a first one of the plurality of TAP controllers.